Appendix B – Micron Technology's Supplemental Response to Interrogatory No. 5

INVALIDITY OF THE '105 PATENT

Claims of the '105 Patent	Grounds for Invalidity
31. A synchronous memory device having at least one memory section which includes a plurality of memory cells, the memory device comprises: internal clock generation circuitry to generate a first internal clock signal and a second internal clock signal, wherein the internal clock generation circuit generates the first and second internal clock signals using at least a first external clock; an output driver, coupled to the internal clock generation circuitry, the output driver outputs data on a bus in response to the first and second internal clock signals and synchronously with respect to at least the first external clock signal.	**1. Grounds for Invalidity Under Rambus's Infringement Contentions:** Under Rambus's infringement contentions, this claim is invalid as anticipated and/or rendered obvious by many prior art references, including without limitation the Redwine, Aichelmann, Chin, and Tam references.[1] To the extent that Rambus's infringement contentions are premised on the term "bus" as not being limited to a multiplexed bus, the claim is also invalid under § 112 ¶ 1 for failure to meet the written description requirement. **2. Grounds for Invalidity Under the Virginia Court's Claim Construction of the "bus" and "request" claim terms:** Alternatively, under the Virginia Court's claim construction, this claim is invalid as rendered obvious by many prior art references, taken singly or in combination, including without limitation, the combinations of any prior art reference taken from Group I below with any other prior art reference taken from Group II below: • Group I: Redwine, Aichelmann, Chin, Tam • Group II: Hoff, Fischer, MIPS R6020, Bomba, Penzel. Jackson **3. Additional § 112 ¶ 1 Grounds for Invalidity Under Either Rambus's Infringement Contentions or the Virginia Court's Claim Construction:** The claim is also invalid under § 112 ¶ 1 (written description, enablement) under either Rambus's infringement contentions or the Virginia Court's claim construction because there is no written support in the description for a claim that does not use the disclosed clock averaging feature (Figs 8a/b and 12 of the patent specification), and/or because there is no disclosure of the use of a single clock signal transmitted as a single ended signal or differentially.

[1] See Attachment A for complete citations of all prior art references listed in this Appendix.

Claims of the '105 Patent	Grounds for Invalidity
34. The memory device of claim 31 further including clock receiver circuitry to receive the first external clock and wherein the internal clock generation circuitry includes delay locked loop circuitry, coupled to the clock receiver circuitry, to generate the first internal clock signal and the second internal clock signal using at least the first external clock.	**1. Gr unds for Invalidity Under Rambus's Infringement Contentions:** Under Rambus' infringement contentions, this claim is invalid as anticipated and/or rendered obvious by many prior art references, taken singly (e.g., SCI, MC88200, Uvieghara, Johnson, Wiggers) or in combination, including without limitation the combinations of a prior art reference taken from Group I below with another prior art reference taken from Group II below: • Group I: Redwine, Aichelmann, Chin, Tam • Group II: Flora, Uvieghara, Johnson I, Johnson II, Johnson III, MIPS R2010, MIPS R3010, Grover, Wiggers, Lofgren, SCI, MC88200 Same grounds of invalidity under § 112 ¶ 1 as in the independent claim. **2. Grounds for Invalidity Under the Virginia Court's Claim Construction of the "bus" and "request" claim terms:** Under the Virginia Court's claim construction, this claim is invalid as rendered obvious by many prior art references, taken singly or in combination, including without limitation, any combination of three prior art references, each taken respectively from one of the Groups I, II or III below: • Group I: Redwine, Aichelmann, Chin, Tam • Group II: Flora, Uvieghara, Johnson I, Johnson II, Johnson III, MIPS R2010, MIPS R3010, Grover, Wiggers, Lofgren, SCI, MC88200 • Group III: Hoff, Fischer, MIPS R6020, Bomba, Penzel, Jackson **3. Additional § 112 ¶ 1 Grounds for Invalidity Under Either Rambus's Infringement Contentions or the Virginia Court's Claim Construction:** The claim is also invalid under § 112 ¶ 1 (written description, enablement) because the clock averaging feature (disclosed in Figs 8a/b and 12 of the patent specification) is not claimed, there is no disclosure of the use of a single clock signal transmitted as a single-ended signal or differentially, and/or because there is no disclosure of a "delay locked loop."

Claims f the '105 Patent	Grounds f r Invalidity
36. A synchronous memory device having at least one memory section which includes a plurality of memory cells, wherein the memory device receives first and second external clock signals and outputs data on a bus, the memory device comprises: a plurality of output drivers, each output driver being coupled to the bus to output data on the bus synchronously with respect to the first and second external clock signals.	**1. Grounds for Invalidity Under Rambus's Infringement Contentions:** This claim is invalid as anticipated and/or rendered obvious by many prior art references, taken singly or in combination, including without limitation, the Hoff, Fischer, Bomba, Uvieghara, SCI and Gigabit references. To the extent that Rambus's infringement contentions are premised on the term "bus" as not being limited to a multiplexed bus, the claim is also invalid under § 112 ¶ 1 for failure to meet the written description requirement. **2. Grounds for Invalidity Under the Virginia Court's Claim Construction of the "bus" and "request" claim terms:** The claim is also invalid under § 112 ¶ 1 (written description, enablement) under either Rambus's infringement contentions or the Virginia Court's claim construction because there is no written support in the description for a claim that does not use the disclosed clock averaging feature (Figs 8a/b and 12 of the patent specification), and/or because there is no disclosure of the use of a single clock signal transmitted differentially. Furthermore, the claim is invalid under § 112 ¶ 2 because the claim limitation "synchronously with respect to the first and second external clock signals" is indefinite.
37. The memory device of claim 36 further including internal clock generation circuitry which generates first and second internal clock signals using the first and second external clock signals, and wherein the plurality of output drivers output data on the bus in response to the first internal clock signal and the second internal clock signal.	This claim is invalid as anticipated and/or rendered obvious by many prior art references, taken singly or in combination, including without limitation, the Hoff, Fischer, Bomba, Uvieghara, SCI and Gigabit references, as well as the combination of any of these references with any one of the following references: Aichelmann, Redwine, Tam or Chin. Same grounds for invalidity under § 112 ¶1 as in the independent claim.
40. The memory device of claim 36 further including clock receiver circuitry to receive the first and second external clock signals, and wherein the memory device further includes delay locked loop circuitry, coupled to the clock receiver circuitry, to generate first and second internal clock signals.	**1. Grounds for Invalidity Under Rambus's Infringement C ntenti ns:** Under Rambus' infringement allegations, this claim is invalid as anticipated or rendered obvious by many prior art references, taken singly (e.g., SCI,

Claims f the '105 Patent	Gr unds for Invalidity
	Uvieghara) or in combination, including without limitation, any combination of a prior art reference taken from Group I below with a prior art reference taken from Group II below: • Group I: Aichelmann, Redwine, Chin, Gigabit, Bomba, Fischer • Group II: Flora, Uvieghara, Johnson I, Johnson II, Johnson III, MIPS R2010, MIPS R3010, Grover, Wiggers, Lofgren, SCI, MC88200 Same grounds for invalidity under § 112 ¶ 1 as in the independent claim. **2. Grounds for Invalidity Under the Virginia Court's Claim Construction of the "bus" and "request" claim terms:** Under the Virginia Court's claim construction, this claim is invalid as rendered obvious by many prior art references, taken singly or in combination, including without limitation, any combination of prior art references, each taken from one of the Groups I, II or III below: • Group I: Aichelmann, Redwine, Chin, Gigabit, Bomba, Fischer • Group II: Flora, Uvieghara, Johnson I, Johnson II, Johnson III, MIPS R2010, MIPS R3010, Grover, Wiggers, Lofgren, SCI, MC88200 • Group III: Hoff, Fischer, MIPS R6020 , Bomba, Penzel, Jackson **3. Additional § 112 ¶ 1 Grounds for Invalidity Under Either Rambus's Infringement Contentions or the Virginia Court's Claim Construction:** The claim is also invalid under § 112 ¶ 1 (written description, enablement) because the clock averaging feature (Figs 8a/b and 12 of the patent specification) is not claimed, there is no disclosure of the use of a single clock signal transmitted differentially, and/or because there is no disclosure of a "delay locked loop."

INVALIDITY OF THE '263 PATENT

Claims f the '263 Patent	Grounds for Invalidity
1. A synchronous semiconductor memory device having at least one memory section which includes a plurality of memory cells, the memory device comprises: a programmable register to store a value which is representative of a delay time after which the memory device responds to a read request.	**1. Grounds f r Invalidity Under Rambus's Infringement Contentions:** Under Rambus' infringement contentions, this claim is invalid as anticipated and/or rendered obvious by many prior art references, including without limitation the Saccardi, Gigabit, Bajwa, Kawamesa, Hasegawa, White and Yamaguchi references. To the extent that Rambus's infringement contentions are premised on the term "bus" as not being limited to a multiplexed bus, the claim is also invalid under § 112 ¶ 1 for failure to meet the written description requirement.. **2. Grounds for Invalidity Under the Virginia Court's Claim Construction of the "bus" and "request" claim terms:** Alternatively, under the Virginia Court's claim construction, this claim is invalid as rendered obvious by many prior art references, taken singly or in combination, including without limitation, the combinations of any prior art reference taken from Group I below with any other prior art reference taken from Group II below: • Group I: Saccardi, Gigabit, Bajwa, Kawamesa, Hasegawa, Yamaguchi, White • Group II: Hoff, Fischer, MIPS R6020, Bomba, Penzel, Jackson
2. The synchronous memory device of claim 1 further including output drivers, coupled to an external bus, to output data on the bus, in response to the read request, synchronously with respect to an external clock.	Same grounds as discussed for claim 1.
3. The synchronous memory device of claim 2 wherein the value is representative of a number of clock cycles of the external clock.	Same grounds as discussed for claim 1.
4. The synchronous memory device of claim 1 wherein, during an initialization sequence, the programmable register stores the value.	Same grounds as discussed for claim 1.
5. The synchronous semiconductor memory device of claim 1 wherein, in response to a control register access, the programmable register stores the value.	Same grounds as discussed for claim 1.
14. A synchronous semiconductor memory device having at least one memory section which includes a plurality of memory cells, the memory device comprising: a programmable register to store a value which is representative of a number of clock cycles of an	Same grounds as discussed for claim 1.

Claims of the '263 Patent	Grounds for Invalidity
external clock to transpire before data is output onto an external bus in response to a read request; and a plurality of output drivers, coupled to the bus, to output data in response to the read request, wherein the output drivers output data on the bus after the number of clock cycles of the external clock transpire.	
16. The synchronous memory device of claim 14 wherein, during an initialization sequence, the programmable register stores the value.	Same grounds as discussed for claim 1.
17. The synchronous semiconductor memory device of claim 14 wherein, in response to a control register access, the programmable register stores the value.	Same grounds as discussed for claim 1.
18. A method of controlling the operation of a synchronous semiconductor memory device wherein the memory device includes a register, the method comprising: providing a time delay value to the memory device; storing the time delay value in the register in the memory device, wherein the time delay value is representative of a time delay after which the memory device responds to a transaction request.	Same grounds as discussed for claim 1.
19. The method of claim 18 further including issuing a control register access wherein, in response to the control register access, the memory device stores a time delay value in the register.	Same grounds as discussed for claim 1.
21. The method of claim 18 further including initializing the register by providing a time delay value to the memory device after issuing a control register access.	Same grounds as discussed for claim 1.
23. The method of claim 18 further including initializing the register after the memory device is powered-up or reset.	Same grounds as discussed for claim 1.
24. The method of claim 18 further including selecting one of a plurality of time delays after which the memory device is to provide data in response to a read request.	Same grounds as discussed for claim 1.
25. The method of claim 18 wherein the transaction request is a read request.	Same grounds as discussed for claim 1.
27. A method of operation of a semiconductor memory device wherein the memory device includes a programmable register, the method	Same grounds as discussed for claim 1.

Claims of the '263 Patent	Grounds for Invalidity
comprising: receiving a time delay value, wherein the time delay value is representative of a number of clock cycles of an external clock to transpire before data is output onto an external bus in response to a read request; and storing the time delay value in the register.	
28. The method of claim 27 further including receiving a control register access wherein, in response to the the register stores the time delay value.	Same grounds as discussed for claim 1. Further, this claim is invalid for indefiniteness under § 112 ¶ 2.
30. An integrated circuit device having memory including at least one memory section which includes a plurality of memory cells, the integrated circuit device comprising: a programmable register to store a value which is representative of a number of clock cycles of a clock to transpire before data is output onto a bus in response to a read request; and a plurality of output drivers, coupled to the bus, to output data in response to the read request, wherein the output drivers output data on the bus after the number of clock cycles of the clock transpire and synchronously with respect to the clock.	Same grounds as discussed for claim 1.
32. The integrated circuit device of claim 30 wherein, during an initialization sequence, the programmable register stores the value.	Same grounds as discussed for claim 1.
33. The integrated circuit device of claim 30 wherein the integrated circuit device stores the value in the register in response to a control register access.	Same grounds as discussed for claim 1.

INVALIDITY OF THE '804 PATENT

Claims f the '804 Patent	Gr unds for Invalidity
26. An integrated circuit device having at least one memory section which includes a plurality of memory cells, wherein the integrated circuit device outputs data on an external bus synchronously with respect to first and second external clock signals, the integrated circuit device comprises: a first internal register to store a value which is representative of a number of clock cycles to transpire before the integrated circuit device responds to a read request; delay locked loop circuitry to generate an internal clock signal using the first and second external clock signals; and interface circuitry, coupled to the external bus to receive a read request, the interface circuitry includes a plurality of output drivers, coupled to the external bus, to output data on the external bus in response to the internal clock signal, synchronously with respect to the first and second external clock signals and in accordance with the value stored in the first internal register.	**1. Grounds for Invalidity Under Rambus's Infringement Contentions:** Under Rambus' infringement contentions, this claim is invalid as rendered obvious by many prior art references, taken singly or in combination, including the combination of any prior art reference from Group I below with any prior art reference from Group II below: • Group I: Saccardi, Gigabit, Bajwa, Kawamesa, Hasegawa, Yamaguchi, White • Group II: Grover, Flora, Uvieghara, Johnson I, Johnson II, Johnson III, MIPS R2010, MIPS R3010, Wiggers, Lofgren, SCI, MC88200 To the extent that Rambus's infringement contentions are premised on the term "bus" as not being limited to a multiplexed bus, the claim is also invalid under § 112 ¶ 1 for failure to meet the written description requirement. **2. Grounds for Invalidity Under the Virginia Court's Claim Construction of the "bus" and "request" claim terms:** Alternatively, under the Virginia Court's claim construction, this claim is invalid as rendered obvious by many prior art references, taken singly or in combination, including without limitation, any combination of three prior art references, each taken respectively from one of the Groups I, II or III below: • Group I: Saccardi, Gigabit, Bajwa, Kawamesa, Hasegawa, Yamaguchi, White • Group II: Grover, Flora, Uvieghara, Johnson I, Johnson II, Johnson III, MIPS R2010, MIPS R3010, Wiggers, Lofgren, SCI, MC88200 • Group III: Hoff, Fischer, MIPS R6020, Bomba, Penzel, Jackson **3. Additional § 112 ¶ 1 Grounds for Invalidity Under Either Rambus's Infringement Contentions or the Virginia Court's Claim Construction:** The claim is also invalid under § 112 ¶ 1 (written description, enablement) because the clock averaging feature (disclosed in Figs 8a/b and 12 of the patent specification) is not claimed, there is no disclosure of the use of a single clock signal

Claims f the '804 Patent	Gr unds f r Invalidity
	transmitted differentially, and/or because there is no disclosure of a "delay locked loop."

INVALIDITY OF THE '443 PATENT

Claims of the '443 Patent	Grounds for Invalidity
1. A synchronous memory device having a memory cell array divided into a plurality of subarrays, wherein each subarray includes a plurality of subarray sections, the memory device comprising: clock receiver circuitry to receive an external clock signal from an external bus; clock generation circuitry, coupled to the clock receiver circuitry, to generate a first internal clock signal having a clock edge which is synchronized with the external clock signal and to generate a second internal clock signal having a clock edge which is synchronized with the external clock signal and to generate a second internal clock signal having a clock edge which is synchronized with the external clock signal; a first subarray section having a first internal I/O line to access data from a first memory cell location and a second internal I/O line to access data from a second memory cell location, wherein the first and second memory cell locations are in the first subarray section; a second subarray section having a first internal I/O line to access data from a third memory cell location and a second internal I/O line to access data from a fourth memory cell location, wherein the third and fourth memory cell locations are in the second subarray section; output driver circuitry, including a first output driver and a second output driver, to output data onto the external bus in response to a read request; and multiplexer circuitry, coupled to the output driver circuitry, wherein: the multiplexer circuitry couples the first internal I/O line of the first subarray section to an input of the first output driver and couples the first internal I/O line of the second subarray section to an input of the second output driver in response to the clock edge of the first internal clock signal; and the multiplexer circuitry couples the second internal I/O line of the first subarray section to an input of the first output driver and couples the second internal I/O line of the second subarray section to an input of the second out driver in response to the clock edge of the second internal clock signal.	**1. Grounds for Invalidity Under Rambus's Infringement Contentions:** Under Rambus' infringement contentions, this claim is invalid as anticipated and/or rendered obvious by many prior art references, including without limitation the Redwine, Aichelmann or Chin references. To the extent that Rambus's infringement contentions are premised on the term "bus" as not being limited to a multiplexed bus, the claim is also invalid under § 112 ¶ 1 for failure to meet the written description requirement. **2. Grounds for Invalidity Under the Virginia Court's Claim Construction of the "bus" and "request" claim terms:** Alternatively, under the Virginia Court's claim construction, this claim is invalid as rendered obvious by many prior art references, taken singly or in combination, including without limitation, the combinations of any prior art reference taken from Group I below with any other prior art reference taken from Group II below: • Group I: Redwine, Aichelmann, Chin • Group II: Hoff, Fischer, MIPS R6020, Bomba, Penzel, Jackson **3. Additional § 112 ¶ 1 Grounds for Invalidity Under Either Rambus's Infringement Contentions or the Virginia Court's Claim Construction:** The claim is also invalid under § 112 ¶ 1 (written description, enablement) under either Rambus's infringement contentions or the Virginia Court's claim construction because there is no written support in the description for a claim that does not use the disclosed clock averaging feature (Figs 8a/b and 12 of the patent specification), and/or because there is no disclosure of the use of a single clock signal transmitted differentially.
3. The memory device of claim 1 wherein the first internal clock signal is generated by a delay locked loop.	**1. Grounds for Invalidity Under Rambus's Infringement Contentions:** Under Rambus' infringement contentions, this claim is invalid as rendered obvious by any combinati n of a prior art reference taken from Group I below with another prior art reference taken from Group II

Claims f the '443 Patent	Grounds f r Invalidity
	below: • Group I: Redwine, Aichelmann, Chin • Group II: Flora, Uvieghara, Johnson I, Johnson II, Johnson III, MIPS R2010, MIPS R3010, Grover, Wiggers, Lofgren, SCI, MC88200 Same grounds for invalidity under § 112 ¶ 1 as in the independent claim. **2. Grounds for Invalidity Under the Virginia Court's Claim Construction of the "bus" and "request" claim terms:** Under the Virginia Court's claim construction, this claim is invalid as rendered obvious by many prior art references, taken singly or in combination, including without limitation, any combination of three prior art references, each taken respectively from one of the Groups I, II or III below: • Group I: Redwine, Aichelmann, Chin • Group II: Flora, Uvieghara, Johnson I, Johnson II, Johnson III, MIPS R2010, MIPS R3010, Grover, Wiggers, Lofgren, SCI, MC88200 • Group III: Hoff, Fischer, MIPS R6020, Bomba, Penzel, Jackson **3. Additional § 112 ¶ 1 Grounds for Invalidity Under Either Rambus's Infringement Contentions or the Virginia Court's Claim Construction:** The claim is also invalid under § 112 ¶ 1 (written description, enablement) because the clock averaging feature (disclosed in Figs 8a/b and 12 of the patent specification) is not claimed, there is no disclosure of the use of a single clock signal transmitted as a single-ended signal or differentially, and/or because there is no disclosure of a "delay locked loop."
6. The memory device of claim 1 further including an internal register for storing a value indicative of a number of clock cycles of the external clock signal to transpire before data is driven onto the external bus in response to a read request.	**1. Grounds for Invalidity Under Rambus's Infringement Contentions:** Under Rambus' infringement contentions, this claim is invalid as rendered obvious by any combination of a prior art reference taken from Group I below with another prior art reference taken from Group II below: • Group I: Redwine, Aichelmann, Chin • Group II: Saccardi, Gigabit, Bajwa, Kawamesa, Hasegawa, Yamaguchi, White

Claims of the '443 Patent	Grounds for Invalidity
	Same grounds for invalidity under § 112 ¶ 1 as in the independent claim. **2. Grounds for Invalidity Under the Virginia Court's Claim Construction of the "bus" and "request" claim terms:** Under the Virginia Court's claim construction, this claim is invalid as rendered obvious by many prior art references, taken singly or in combination, including without limitation, any combination of three prior art references, each taken respectively from one of the Groups I, II or III below: • Group I: Redwine, Aichelmann, Chin • Group II: Saccardi, Gigabit, Bajwa, Kawamesa, Hasegawa, Yamaguchi, White • Group III: Hoff, Fischer, MIPS R6020, Bomba, Penzel, Jackson Same grounds for invalidity under § 112 ¶ 1 as in the independent claim.
8. The memory device of claim 1 further including a first plurality of sense amplifiers and a second plurality of sense amplifiers, wherein: data accessed from a first memory cell location is latched in a sense amplifier of the first plurality of sense amplifiers and data accessed from the second memory cell location is latched in a sense amplifier of the second plurality of sense amplifiers; and data accessed from a third memory cell location is latched in a sense amplifier of the first plurality of sense amplifiers and data accessed from the fourth memory cell location is latched in a sense amplifier of the second plurality of sense amplifiers.	Same grounds as discussed for claim 1.
11. The memory device of claim 1 wherein the first subarray section is automatically precharged after executing the read request.	**1. Grounds for Invalidity Under Rambus's Infringement Contentions:** Under Rambus' infringement contentions, this claim is invalid as anticipated as rendered obvious by many references, taken singly (e.g., Chin) or in combination, including without limitation any combination of a prior art reference taken from Group I below with another prior art reference taken from Group II below: • Group I: Redwine, Aichelmann, Chin • Group II: Bajwa, Chin, Chappell Same grounds for invalidity under § 112 ¶ 1 as in the independent claim. **2. Gr unds f r Invalidity Under the Virginia**

Claims of the '443 Patent	Grounds for Invalidity
	Court's Claim Constructi n f the "bus" and "request" claim terms: Under the Virginia Court's claim construction, this claim is invalid as rendered obvious by many prior art references, taken singly or in combination, including without limitation, any combination of three prior art references, each taken respectively from one of the Groups I, II or III below: • Group I: Redwine, Aichelmann, Chin • Group II: Bajwa, Chin • Group III: Hoff, Fischer, MIPS R6020, Bomba, Penzel, Jackson Same grounds for invalidity under § 112 ¶ 1 as in the independent claim.
13. The memory device of claim 12 wherein the data latched in the plurality of sense amplifiers is maintained in the sense amplifiers for a subsequent read request.	Same grounds as discussed for claim 1.
16. The memory device of claim 1 wherein the external clock signal has a fixed frequency.	Same grounds as discussed for claim 1.
18. The memory device of claim 1 wherein the output driver circuitry outputs a predetermined amount of data defined by block size information and wherein the block size information is a binary code.	This claim is invalid as rendered obvious by combinations of any prior art reference taken from Group I below with any other prior art reference taken from Group II below: • Group I: Redwine, Aichelmann, Chin • Group II: MIPS R6020, Fischer, Bomba, Jackson, Penzel, Bajwa, SCI, MC88200 Same grounds for invalidity under § 112 ¶ 1 as in the independent claim.1
21. A synchronous memory device having a memory cell array divided into a plurality of subarrays, including a first subarray and a second subarray wherein each subarray includes a plurality of subarray sections, the memory device comprises: clock receiver circuitry to receive an external clock signal from an external bus; clock generation circuitry, coupled to the clock receiver circuitry, to generate a first internal clock signal having a clock edge which is synchronized with the external clock signal and to generate a second internal clock signal having a clock edge which is synchronized with the external clock signal; a first subarray section of a first subarray, the first subarray section of a first subarray, the first subarray section having a first internal I/O line to access data from a first memory cell location and a second internal I/O line to access data from a second memory cell locati n, wherein the first and	**1. Grounds for Invalidity Under Rambus's Infringement Contentions:** Under Rambus' infringement contentions, this claim is invalid as anticipated and/or rendered obvious by many prior art references, including without limitation the Redwine, Aichelmann or Chin references. To the extent that Rambus's infringement contentions are premised on the term "bus" as not being limited to a multiplexed bus, the claim is also invalid under § 112 ¶ 1 for failure to meet the written description requirement. **2. Grounds for Invalidity Under the Virginia m P pup** **Ă** **Âþ Âþ** **Âþ Â þ**

Claims f the '443 Patent	Grounds for Invalidity
second memory cell locations are in the first subarray section; a second subarray section of a second subarray, the second subarray section having a first internal I/O line to access data from a third memory cell location and a second internal I/O line to access data from a fourth memory cell location, wherein the third and fourth memory cell locations are in the second subarray section; output driver circuitry, including a first output driver and a second output driver, to output data onto the external bus in response to a read request; and multiplexer circuitry, coupled to the output driver circuitry, wherein: the multiplexer circuitry couples the first internal I/O line of the first subarray section to an input of the first output driver and couples the first internal I/O line of the second subarray section to an input of the second output driver in response to the clock edge of the first internal clock signal; and the multiplexer circuitry couples the second internal I/O line of the first subarray section to an input of the first output driver and couples the second internal I/O line of the second subarray section to an input of the second output driver in response to the clock edge of the second internal clock signal.	Alternatively, under the Virginia Court's claim construction, this claim is invalid as rendered obvious by many prior art references, taken singly or in combination, including without limitation, the combinations of any prior art reference taken from Group I below with any other prior art reference taken from Group II below: • Group I: Redwine, Aichelmann, Chin • Group II: Hoff, Fischer, MIPS R6020, Bomba, Penzel, Jackson **3. Additional § 112 ¶ 1 Grounds for Invalidity Under Either Rambus's Infringement Contentions or the Virginia Court's Claim Construction:** The claim is also invalid under § 112 ¶ 1 (written description, enablement) under either Rambus's infringement contentions or the Virginia Court's claim construction because there is no written support in the description for a claim that does not use the disclosed clock averaging feature (Figs 8a/b and 12 of the patent specification), and/or because there is no disclosure of the use of a single clock signal transmitted differentially.
22. The memory device of claim 21 wherein the first internal clock signal is generated by a delay locked loop.	Same grounds as discussed for claim 3.
29. A memory system having a synchronous memory device coupled to a bus, the memory device having a memory cell array divided into a plurality of subarrays, wherein each subarray includes a plurality of subarray sections, the memory system comprises: clock receiver circuitry to receive a bus clock from the bus; clock generation circuitry to generate a first clock edge which is synchronized with the bus clock and to generate a second clock edge which is synchronized with the bus clock; a first subarray section having a first data line to access data from a first memory cell location and a second data line to access data from a second memory cell location, wherein the first and second memory cell locations are in the first subarray section; a second subarray section having a first data line to access data from a third memory cell location and a second data line to access data from a fourth memory cell location, wherein the third and fourth memory cell locations are in the second subarray secti n;	**1. Grounds for Invalidity Under Rambus's Infringement Contentions:** Under Rambus' infringement contentions, this claim is invalid as anticipated and/or rendered obvious by many prior art references, including without limitation the Redwine, Aichelmann or Chin references. To the extent that Rambus's infringement contentions are premised on the term "bus" as not being limited to a multiplexed bus, the claim is also invalid under § 112 ¶ 1 for failure to meet the written description requirement. **2. Grounds for Invalidity Under the Virginia Court's Claim Construction of the "bus" and "request" claim terms:** Alternatively, under the Virginia Court's claim construction, this claim is invalid as rendered obvious by many prior art references, taken singly or in combination, including without limitation, the combinations of any prior art reference taken from

Claims of the '443 Patent	Gr unds for Invalidity
output drivers, including a first output driver and a second output driver, to output a predetermined amount of data onto the bus in response to a read request; and multiplexer circuitry, coupled to the output drivers, wherein: the multiplexer circuitry couples the first data line of the first subarray section to an input of the first output driver and couples the first data line of the second subarray section to an input of the second output driver in response to the first clock edge; and the multiplexer circuitry couples the second data line of the first subarray section to an input of the first output driver and couples the second data line of the second subarray section to an input of the second output driver in response to the second clock edge.	Group I below with any other prior art reference taken from Group II below: • Group I: Redwine, Aichelmann, Chin • Group II: Hoff, Fischer, MIPS R6020, Bomba, Penzel, Jackson **3. Additional § 112 ¶ 1 Grounds for Invalidity Under Either Rambus's Infringement Contentions or the Virginia Court's Claim Construction:** The claim is also invalid under § 112 ¶ 1 (written description, enablement) under either Rambus's infringement contentions or the Virginia Court's claim construction because there is no written support in the description for a claim that does not use the disclosed clock averaging feature (Figs 8a/b and 12 of the patent specification), and/or because there is no disclosure of the use of a single clock signal transmitted differentially.
30. The memory system of claim 29 wherein clock generation circuitry includes a delay locked loop.	**1. Grounds for Invalidity Under Rambus's Infringement Contentions:** Under Rambus' infringement contentions, this claim is invalid as rendered obvious by any combination of a prior art reference taken from Group I below with another prior art reference taken from Group II below: • Group I: Redwine, Aichelmann, Chin • Group II: Flora, Uvieghara, Johnson I, Johnson II, Johnson III, MIPS R2010, MIPS R3010, Grover, Wiggers, Lofgren, SCI, MC88200 Same grounds for invalidity under § 112 ¶ 1 as in the independent claim. **2. Grounds for Invalidity Under the Virginia Court's Claim Construction of the "bus" and "request" claim terms:** Under the Virginia Court's claim construction, this claim is invalid as rendered obvious by many prior art references, taken singly or in combination, including without limitation, any combination of three prior art references, each taken respectively from one of the Groups I, II or III below: • Group I: Redwine, Aichelmann, Chin • Group II: Flora, Uvieghara, Johnson I, Johnson II, Johnson III, MIPS R2010, MIPS R3010, Grover, Wiggers, Lofgren, SCI, MC88200

Claims of the '443 Patent	Grounds f r Invalidity
	• Group III: Hoff, Fischer, MIPS R6020, Bomba, Penzel, Jackson **3. Additional § 112 ¶ 1 Grounds for Invalidity Under Either Rambus's Infringement Contentions or the Virginia Court's Claim Construction:** The claim is also invalid under § 112 ¶ 1 (written description, enablement) because the clock averaging feature (disclosed in Figs 8a/b and 12 of the patent specification) is not claimed, there is no disclosure of the use of a single clock signal transmitted as a single-ended signal or differentially, and/or because there is no disclosure of a "delay locked loop."
31. The memory system of claim 29 further including a register for storing bus clock information indicative of a number of clock cycles of the bus clock to transpire before data is driven onto the bus in response to a read request wherein the bus clock information represents a fraction or a whole number of clock cycles of the bus clock.	**1. Grounds for Invalidity Under Rambus's Infringement Contentions:** Under Rambus' infringement contentions, this claim is invalid as rendered obvious by any combination of a prior art reference taken from Group I below with another prior art reference taken from Group II below: • Group I: Redwine, Aichelmann, Chin • Group II: Saccardi, Gigabit, Bajwa, Kawamesa, Hasegawa, Yamaguchi, White Same grounds for invalidity under § 112 ¶ 1 as in the independent claim. **2. Grounds for Invalidity Under the Virginia Court's Claim Construction of the "bus" and "request" claim terms:** Under the Virginia Court's claim construction, this claim is invalid as rendered obvious by many prior art references, taken singly or in combination, including without limitation, any combination of three prior art references, each taken respectively from one of the Groups I, II or III below: • Group I: Redwine, Aichelmann, Chin • Group II: Saccardi, Gigabit, Bajwa, Kawamesa, Hasegawa, Yamaguchi, White • Group III: Hoff, Fischer, MIPS R6020, Bomba, Penzel, Jackson Same grounds for invalidity under § 112 ¶ 1 as in the independent claim.
32. The memory system of claim 29 wherein the bus is external to the memory device.	Same grounds as discussed for claim 29.

INVALIDITY OF THE '214 PATENT

Claims of the '214 Patent	Gr unds f r Invalidity
1. A method of operating a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method comprising: providing first block size information to the memory device, wherein the first block size information defines a first amount of data to be output onto a bus in response to a read request; and issuing a first read request to the memory device, wherein in response to the first read request, the memory device outputs the first amount of data onto the bus synchronously with respect to a first and a second external clock signal wherein a first portion of the first amount of data is output synchronously with respect to the first external clock signal and a second portion of the first amount of data is output synchronously with respect to the second external clock signal.	This claim is invalid as anticipated or rendered obvious by many prior art references, including SCI, MIPS R6020, Bajwa, Fischer, Bomba, Penzel, Jackson, and/or rendered obvious by combining any one of the above cited references with Aichelmann, Redwine or Chin. To the extent that Rambus's infringement contentions are premised on the term "bus" as not being limited to a multiplexed bus, the claim is also invalid under § 112 ¶ 1 for failure to meet the written description requirement. The claim is also invalid under § 112 ¶ 1 (written description, enablement) because there is no written support in the description for a claim that does not use the disclosed clock averaging feature (Figs 8a/b and 12 of the patent specification), and/or because there is no disclosure of the use of a single clock signal transmitted differentially. The claim is also invalid under § 112 ¶ 2 because the claim limitation "synchronously with respect to a first and a second external clock signal" is indefinite.
2. The method of claim 1 further including issuing a second read request to the memory device, wherein in response to the second read request, the memory device outputs the first amount of data onto the bus synchronously with respect to the first and second external clock signals wherein the first portion of the first amount of data is output synchronously with respect to the first external clock signal and the second portion of the first amount of data is output synchronously with respect to the second external clock signal.	Same grounds as discussed for claim 1.
4. The method of claim 1 further including providing a code which is representative of a number of clock cycles of the first and second external clock signals to transpire before data is output by the memory device onto the bus wherein the memory device stores the code in a programmable register on the memory device, and wherein the first amount of data corresponding to the first block size information is output after the number of clock cycles transpire.	This claim is invalid as anticipated or rendered obvious by the Bajwa reference and by any combination of a prior art reference taken from Group I below with another prior art reference taken from Group II below: • Group I: SCI, MIPS R6020, Bajwa, Fischer, Bomba, Penzel, Jackson • Group II: Saccardi, Gigabit, Bajwa, Kawamesa, Hasegawa, Yamaguchi, White The claim is also rendered obvious by further combining any of the above prior art combinations with Aichelmann, Redwine or Chin.

Claims of the '214 Patent	Grounds for Invalidity
	Same grounds for invalidity under § 112 ¶ 1 as in the independent claim.
6. The method of claim 1 wherein the first block size information is a binary code indicative of the first amount of data to be output in response to the read request.	Same grounds as discussed for claim 1.
9. The method of claim 1 wherein the first amount of data corresponding to the first block size information is output during a plurality of clock cycles of the first and second external clock signals.	Same grounds as discussed for claim 1.
10. The method of claim 1 further including generating at least one internal clock signal using the first and second external clock signals wherein the first amount of data corresponding to the first block size information is output onto the bus synchronously with respect to at least one internal clock signal.	Same grounds as discussed for claim 1.
11. The method of claim 10 further including a delay locked loop to generate the at least one internal clock signal using the first and the second external clock signals.	This claim is invalid as anticipated or rendered obvious by the SCI reference, and is also rendered obvious by any combination of a prior art reference taken from Group I below with another prior art reference taken from Group II below: • Group I: SCI, MIPS R6020, Bajwa, Fischer, Bomba, Penzel, Jackson • Group II: Grover, Wiggers, Flora, Lofgren, Johnson I, Johnson II, Johnson III, MIPS R2010, MIPS R3010, SCI, MC88200, Uvieghara The claim is also rendered obvious by further combining any of the above prior art combinations with Aichelmann, Redwine or Chin. Same grounds for invalidity under § 112 ¶ 1 as in the independent claim.
14. The method of claim 1 further including automatically precharging the memory device before executing another read request.	This claim is invalid as anticipated or rendered obvious by the Bajwa reference and is rendered obvious by any combination of a prior art reference taken from Group I below with another prior art reference taken from Group II below: • Group I: SCI, MIPS R6020, Bajwa, Fischer, Bomba, Penzel, Jackson • Group II: Bajwa, Chin, Chappell The claim is also rendered obvious by further combining any of the above prior art combinations with Aichelmann, Redwine or Chin. Same grounds for invalidity under § 112 ¶ 1 as in the independent claim.

Claims of the '214 Patent	Gr unds f r Invalidity
15. A method of operation of a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method comprising: receiving first block size information, wherein the first block size information defines a first amount of data to be output onto a bus in response to a read request; receiving a first read request; and outputting the first amount of data corresponding to the first block size information, in response to the first read request, onto the bus synchronously with respect to a first and a second external clock signal wherein a first portion of the first amount of data is output synchronously with respect to the first external clock signal and a second portion of the first amount of data is output synchronously with respect to the second external clock signal.	This claim is invalid as anticipated or rendered obvious by many prior art references, including SCI, MIPS R6020, Bajwa, Fischer, Bomba, Penzel, Jackson, and/or rendered obvious by combining any one of the above cited references with Aichelmann, Redwine or Chin. To the extent that Rambus's infringement contentions are premised on the term "bus" as not being limited to a multiplexed bus, the claim is also invalid under § 112 ¶ 1 for failure to meet the written description requirement. The claim is also invalid under § 112 ¶ 1 (written description, enablement) because there is no written support in the description for a claim that does not use the disclosed clock averaging feature (Figs 8a/b and 12 of the patent specification), and/or because there is no disclosure of the use of a single clock signal transmitted differentially. The claim is also invalid under § 112 ¶ 2 because the claim limitation "synchronously with respect to a first and a second external clock signal" is indefinite.
16. The method of claim 15 further including: receiving a second read request; and outputting the first amount of data corresponding to the first block size information, in response to the second read request, onto the bus synchronously with respect to the first and second external clock signals wherein a first portion of the second amount of data is output synchronously with respect to the first external clock signal and a second portion of the second amount of data is output synchronously with respect to the second external clock signal.	Same grounds as discussed for claim 15.
18. The method of claim 15 further including storing a code in an access time register, the code being representative of a number of clock cycles of the first and second external clock signals to transpire before data is output onto the bus in response to the first read request, wherein the first amount of data corresponding to the first block size information is output after the number of clock cycles transpire.	This claim is invalid as anticipated or rendered obvious by the Bajwa reference and by any combination of a prior art reference taken from Group I below with another prior art reference taken from Group II below: • Group I: SCI, MIPS R6020, Bajwa, Fischer, Bomba, Penzel, Jackson • Group II: Saccardi, Gigabit, Bajwa, Kawamesa, Has gawa, Yamaguchi, White The claim is also rendered obvious by further

Claims f the '214 Patent	Gr unds for Invalidity
	combining any of the above prior art combinations with Aichelmann, Redwine or Chin. Same grounds for invalidity under § 112 ¶ 1 as in the independent claim.
19. The method of claim 18 wherein the code is stored in the access time register during an initialization operation.	Same grounds as discussed for claim 18.
21. The method of claim 15 wherein the first block size information is a binary code indicative of the first amount of data.	Same grounds as discussed for claim 15.
24. The method of claim 15 wherein the first and second external clock signals have a fixed frequency.	Same grounds as discussed for claim 15.
25. The method of claim 15 further including generating at least one internal clock signal using the first and second external clock signals wherein the first amount of data corresponding to the first block size information is output onto the bus synchronously with respect to at least one internal clock signal.	Same grounds as discussed for claim 15.
26. The method of claim 25 further including generating a first internal clock signal using a delay locked loop and the first and the second external clock signals.	This claim is invalid as anticipated or rendered obvious by the SCI reference, and is also rendered obvious by any combination of a prior art reference taken from Group I below with another prior art reference taken from Group II below: • Group I: SCI, MIPS R6020, Bajwa, Fischer, Bomba, Penzel, Jackson • Group II: Grover, Wiggers, Flora, Lofgren, Johnson I, Johnson II, Johnson III, MIPS R2010, MIPS R3010, SCI, MC88200, Uvieghara The claim is also rendered obvious by further combining any of the above prior art combinations with Aichelmann, Redwine or Chin. Same grounds for invalidity under § 112 ¶ 1 as in the independent claim.
29. The method of claim 15 further including automatically precharging the memory device after executing the first read request.	This claim is invalid as anticipated or rendered obvious by the Bajwa reference and is rendered obvious by any combination of a prior art reference taken from Group I below with another prior art reference taken from Group II below: • Group I: SCI, MIPS R6020, Bajwa, Fischer, Bomba, Penzel, Jackson • Group II: Bajwa, Chin The claim is also rendered obvious by further

Claims f the '214 Patent	Grounds for Invalidity
	combining any of the above prior art combinations with Aichelmann, Redwine or Chin. Same grounds for invalidity under § 112 ¶ 1 as in the independent claim.
30. A method of operation of a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method comprises: storing a code in an access time register, wherein the code is representative of a number of clock cycles of a first and second external clock signals to transpire before data is output onto a bus after receipt of a read request; receiving block size information, wherein the block size information is representative of an amount of data to be output onto the bus in response to a read request; receiving a first read request; outputting the amount of data corresponding to the block size information onto the bus in response to the first read request; receiving a second read request; outputting the amount of data corresponding to the block size information onto the bus in response to the second read request; and wherein a first portion of the amount of data is output synchronously with respect to the first external clock signal and a second portion of the amount of data is output synchronously with respect to the second external clock signal, during a plurality of clock cycles of the first and second external clock signals, after the number of clock cycles transpire.	This claim is invalid as anticipated or rendered obvious by the Bajwa reference and by any combination of a prior art reference taken from Group I below with another prior art reference taken from Group II below: • Group I: SCI, MIPS R6020, Bajwa, Fischer, Bomba, Penzel, Jackson • Group II: Saccardi, Gigabit, Bajwa, Kawamesa, Hasegawa, Yamaguchi, White The claim is also rendered obvious by further combining any of the above prior art combinations with Aichelmann, Redwine or Chin. To the extent that Rambus's infringement contentions are premised on the term "bus" as not being limited to a multiplexed bus, the claim is also invalid under § 112 ¶ 1 for failure to meet the written description requirement. The claim is also invalid under § 112 ¶ 1 (written description, enablement) because there is no written support in the description for a claim that does not use the disclosed clock averaging feature (Figs 8a/b and 12 of the patent specification), and/or because there is no disclosure of the use of a single clock signal transmitted differentially. The claim is also invalid under § 112 ¶ 2 because the claim limitation "synchronously with respect to a first and a second external clock signal" is indefinite.
31. The method of claim 30 wherein the block size information is a binary code indicative of the amount of data.	Same grounds as discussed for claim 30.
36. The method of claim 30 further including storing the code in the access time register during an initialization operation.	Same grounds as discussed for claim 30.

INVALIDITY OF THE '215 PATENT

Claims of the '215 Patent	Grounds for Invalidity
1. A synchronous memory device having a memory cell array having a plurality of subarrays, wherein each subarray includes a plurality of subarray sections, each subarray section includes a plurality of memory cells, the memory device comprising: clock receiver circuitry to receive first and second external clock signals from an external bus; clock generation circuitry, coupled to the clock receiver circuitry, to generate a first internal clock signal having a clock edge which is synchronized with at least the first external clock signal and to generate a second internal clock signal having a clock edge which is synchronized with at least the second external clock signal; a first subarray section, the first subarray section having a first internal I/O line to access data from a first memory cell location and a second internal I/O line to access data from a second memory cell location, wherein the first and second memory cell locations are in the first subarray section; a second subarray section, the second subarray section having a first internal I/O line to access data from a third memory cell location and a second internal I/O line to access data from a fourth memory cell location, wherein the third and fourth memory cell locations are in the second subarray section; output driver circuitry, including a first output driver and a second output driver, to output data onto the external bus in response to a read request; and multiplexer circuitry, coupled to the output driver circuitry, wherein: the multiplexer circuitry couples the first internal I/O line of the first subarray section to an input of the first output driver and couples the first internal I/O line of the second subarray section to an input of the second output driver in response to the clock edge of the first internal clock signal; and the multiplexer circuitry couples the second internal I/O line of the first subarray section to an input of the first output driver and couples the second internal I/O lin of the second subarray section to an	**1. Grounds for Invalidity Under Rambus's Infringement Contentions:** Under Rambus' infringement contentions, this claim is invalid as anticipated and/or rendered obvious by many prior art references, including without limitation, the Redwine, Aichelmann and Chin references. To the extent that Rambus's infringement contentions are premised on the term "bus" as not being limited to a multiplexed bus, the claim is also invalid under § 112 ¶ 1 for failure to meet the written description requirement. **2. Grounds for Invalidity Under the Virginia Court's Claim Construction of the "bus" and "request" claim terms:** Alternatively, under the Virginia Court's claim construction, this claim is invalid as rendered obvious by many prior art references, taken singly or in combination, including without limitation, the combinations of any prior art reference taken from Group I below with any other prior art reference taken from Group II below: • Group I: Redwine, Aichelmann, Chin • Group II: Hoff, Fischer, MIPS R6020, Bomba, Penzel, Jackson **3. Additional § 112 ¶ 1 Grounds for Invalidity Under Either Rambus's Infringement Contentions or the Virginia Court's Claim Construction:** The claim is also invalid under § 112 ¶ 1 (written description, enablement) under either Rambus's infringement contentions or the Virginia Court's claim construction because there is no written support in the description for a claim that does not use the disclosed clock averaging feature (Figs 8a/b and 12 of the patent specification), and/or because there is no disclosure of the use of a single clock signal transmitted differentially.The claim is invalid under § 112 ¶ 2 indefiniteness because of the claim limitation "to generate a first internal clock having a clock edge which is synchronized with at least the first external clock signal and to generate a second internal clock signal having a clock edge which is synchronized with at least the second external clock signal."

Claims of the '215 Patent	Grounds for Invalidity
input of the second output driver in response to the clock edge of the second internal clock signal.	
2. The memory device of claim 1 further including: a register to store a value which is representative of a number of cycles of a first external clock signal to transpire after which the memory device responds to a read request; and wherein the first and second output drivers output data on the external bus after the number of cycles of the first external clock signal have transpired.	**1. Grounds for Invalidity Under Rambus's Infringement Contentions:** Under Rambus' infringement contentions, this claim is invalid as rendered obvious by any combination of a prior art reference taken from Group I below with another prior art reference taken from Group II below: • Group I: Redwine, Aichelmann, Chin • Group II: Saccardi, Gigabit, Bajwa, Kawamesa, Hasegawa, Yamaguchi, White Same grounds for invalidity under § 112 ¶ 1 as in the independent claim. **2. Grounds for Invalidity Under the Virginia Court's Claim Construction of the "bus" and "request" claim terms:** Under the Virginia Court's claim construction, this claim is invalid as rendered obvious by many prior art references, taken singly or in combination, including without limitation, any combination of three prior art references, each taken respectively from one of the Groups I, II or III below: • Group I: Redwine, Aichelmann, Chin • Group II: Saccardi, Gigabit, Bajwa, Kawamesa, Hasegawa, Yamaguchi, White • Group III: Hoff, Fischer, MIPS R6020, Bomba, Penzel, Jackson Same grounds for invalidity under § 112 ¶ 1 as in the independent claim.
3. The memory device of claim 1 wherein the clock generation circuitry further includes a delay locked loop to generate the first internal clock signal using at least the first external clock signal.	**1. Grounds for Invalidity Under Rambus's Infringement Contentions:** Under Rambus' infringement contentions, this claim is invalid as rendered obvious by any combination of a prior art reference taken from Group I below with another prior art reference taken from Group II below: • Group I: Redwine, Aichelmann, Chin • Group II: Flora, Uvieghara, Johnson I, Johnson II, Johnson III, MIPS R2010, MIPS R3010, Grover, Wiggers, Lofgren, SCI, MC88200 Same grounds for invalidity under § 112 ¶ 1 as in the independent claim.

Claims of the '215 Patent	Grounds for Invalidity
	2. Gr unds for Invalidity Under the Virginia Court's Claim Construction of the "bus" and "request" claim terms: Under the Virginia Court's claim construction, this claim is invalid as rendered obvious by many prior art references, taken singly or in combination, including without limitation, any combination of three prior art references, each taken respectively from one of the Groups I, II or III below: • Group I: Redwine, Aichelmann, Chin • Group II: Flora, Uvieghara, Johnson I, Johnson II, Johnson III, MIPS R2010, MIPS R3010, Grover, Wiggers, Lofgren, SCI, MC88200 • Group III: Hoff, Fischer, MIPS R6020, Bomba, Penzel, Jackson0 **3. Additional § 112 ¶ 1 Grounds for Invalidity Under Either Rambus's Infringement Contentions or the Virginia Court's Claim Construction:** The claim is also invalid under § 112 ¶ 1 (written description, enablement) because the clock averaging feature (disclosed in Figs 8a/b and 12 of the patent specification) is not claimed, there is no disclosure of the use of a single clock signal transmitted as a single-ended signal or differentially, and/or because there is no disclosure of a "delay locked loop."
4. The memory device of claim 1 wherein the clock generation circuitry further includes a delay locked loop to generate the first internal clock signal using the first and second external clock signals.	Same grounds as discussed for claim 3.
6. The memory device of claim 1 further including an internal register for storing a value representative of a fraction or whole number of clock cycles of the first external clock signal to transpire before data is driven onto the external bus in response to a read request.	Same grounds as discussed for claim 2.
14. The memory device of claim 1 wherein the output driver circuitry outputs a predetermined amount of data defined by block size information and wherein the block size information is a binary code.	This claim is invalid as rendered obvious by combinations of any prior art reference taken from Group I below with any other prior art reference taken from Group II below: • Group I: Redwine, Aichelmann, Chin • Group II: MIPS R6020, Fischer, Bajwa, SCI, Bomba, Jackson, Penzel, MC88200

Claims of the '215 Patent	Grounds for Invalidity
	Same grounds for invalidity under § 112 ¶ 1 as in the independent claim.
17. A synchronous memory device having a memory cell array divided into a plurality of subarrays, including a first subarray and a second subarray wherein each subarray includes a plurality of subarray sections, the memory device comprises: clock receiver circuitry to receive first and second external clock signals from an external bus; clock generation circuitry, coupled to the clock receiver circuitry, to generate a first internal clock signal having a clock edge which is synchronized with the first external clock signal and to generate a second internal clock signal having a clock edge which is synchronized with the second external clock signal; interface circuitry coupled to the external bus to receive a read request; a first subarray section of a first subarray, the first subarray section having a first internal I/O line to access data from a first memory cell location and a second internal I/O line to access data from a second memory cell location, wherein the first and second memory cell locations are in the first subarray section; a second subarray section of a second subarray, the second subarray section having a first internal I/O line to access data from a third memory cell location and a second internal I/O line to access data from a fourth memory cell location, wherein the third and fourth memory cell locations are in the second subarray section; output driver circuitry, including a first output driver and a second output driver, to output data onto the external bus in response to the read request; and multiplexer circuitry, coupled to the output driver circuitry, wherein: the multiplexer circuitry couples the first internal I/O line of the first subarray section to an input of the first output driver and couples the first internal I/O lin of the second subarray section to an input of the second output driver in response to the clock edge of the first internal clock signal; and	Same grounds as discussed for claim 1.

Claims of the '215 Patent	Grounds for Invalidity
the multiplexer circuitry couples the second internal I/O line of the first subarray section to an input of the first output driver and couples the second internal I/O line of the second subarray section to an input of the second output driver in response to the clock edge of the second internal clock signal.	
18. The memory device of claim 17 further including: a resister to store a value which is representative of a number of cycles of a first external clock signal to transpire after which the memory device responds to a read request; and wherein the first and second output drivers output data on the external bus after the number of cycles of the first external clock signal have transpired.	Same grounds as discussed for claim 2.
19. The memory device of claim 17 wherein the clock generation circuitry further includes a delay locked loop to generate the first internal clock signal using the first and second external clock signals.	Same grounds as discussed for claim 3.

INVALIDITY OF THE '918 PATENT

Claims f the '918 Patent	Gr unds for Invalidity
1. A method of controlling a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of controlling the memory device comprises: providing first block size information to the memory device, wherein the first block size information defines a first amount of data to be output by the memory device onto a bus in response to a read request; and issuing a first read request to the memory device, wherein in response to the first read request, the memory device outputs the first amount of data corresponding to the first block size information onto the bus synchronously with respect to an external clock signal.	This claim is invalid as anticipated and/or rendered obvious by many prior art references, including without limitation the Bajwa, SCI, Fischer, Bomba, Penzel, Jackson, MC88200 and MIPS R6020 references. To the extent that Rambus's infringement contentions are premised on the term "bus" as not being limited to a multiplexed bus, the claim is also invalid under § 112 ¶ 1 for failure to meet the written description requirement.
2. The method of claim 1 wherein first block size information further defines a first amount of data to be input by the memory device from the bus in response to a write request, the method further including issuing a first write request to the memory device wherein, in response to the first write request, the memory device inputs the first amount of data corresponding to the first block size information from the bus synchronously with respect to the external clock signal.	Same grounds as discussed for claim 1.
6. The method of claim 1 further including issuing a second read request to the memory device, wherein in response to the second read request, the memory device outputs the first amount of data corresponding to the first block size information onto the bus synchronously with respect to the external clock signal.	Same grounds as discussed for claim 1.
8. The method of claim 1 further including providing a code which is representative of a delay time to transpire before data is output onto the bus after receipt of a read request, wherein the memory device stores the code in an access time register on the memory device.	This claim is invalid as anticipated and/or rendered obvious by many prior art references, including without limitation the Bajwa reference, and by combinations of a prior art reference taken from Group I below with a prior art reference taken from group II below: • Group I: Bajwa, SCI, Fischer, Bomba, Penzel, Jackson, MC88200 and MIPS R6020 • Group II: Saccardi, Gigabit, Bajwa, Kawamesa, Hasegawa, Yamaguchi, White Same grounds for invalidity under § 112 ¶ 1 as in the independent claim.

Claims of the '918 Patent	Grounds f r Invalidity
9. The method of claim 8 further including receiving the external clock signal wherein the first amount of data corresponding to the first block size information is output in accordance with the delay time.	Same grounds as discussed for claim 8.
13. The method of claim 11 wherein the first block size information is a binary representation of the amount of data to be output after receipt of the first read request.	This claim is invalid as anticipated and/or rendered obvious by many prior art references, including without limitation the SCI, Fischer, Bomba, Penzel, Jackson and MIPS R6020 references. To the extent that Rambus's infringement contentions are premised on the term "bus" as not being limited to a multiplexed bus, the claim is also invalid under § 112 ¶ 1 for failure to meet the written description requirement. The claim is also invalid under § 112 ¶ 1 (written description, enablement) because the clock averaging feature (disclosed in Figs 8a/b and 12 of the patent specification) is not claimed, there is no disclosure of the use of a single clock signal transmitted as a single-ended signal or differentially,
15. The method of claim 11 wherein the external clock signal has a fixed frequency and wherein the first amount of data corresponding to the first block size information is output synchronously during a plurality of clock cycles of the external clock signal.	Same grounds as discussed for claim 13.
16. The method of claim 11 further including generating at least one internal clock signal using the external clock signal wherein the first amount of data corresponding to the first block size information is output onto the bus synchronously with respect to at least one internal clock signal.	Same grounds as discussed for claim 13.
17. The method of claim 16 wherein the internal clock signal is generated by a delay locked loop.	This claim is invalid as anticipated and/or rendered obvious by many prior art references, taken singly (e.g., SCI) or in combination, including without limitation combinations of a prior art reference taken from Group I below with a prior art reference taken from group II below: • Group I: SCI, Fischer, Bomba, Penzel, Jackson, MIPS R6020 • Group II: Flora, Uvieghara, Johnson I, Johnson II, Johnson III, MIPS R2010, MIPS R3010, Grover, Wiggers, Lofgren, SCI, MC88200 To the extent that Rambus's infringement contentions are premised on the term "bus" as not

Claims f the '918 Patent	Grounds for Invalidity
	being limited to a multiplexed bus, the claim is also invalid under § 112 ¶ 1 for failure to meet the written description requirement. The claim is also invalid under § 112 ¶ 1 (written description, enablement) because the clock averaging feature (disclosed in Figs 8a/b and 12 of the patent specification) is not claimed, there is no disclosure of the use of a single clock signal transmitted as a single-ended signal or differentially, and/or because there is no disclosure of a "delay locked loop."
18. A method of operation of a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises: receiving an external clock signal; receiving first block size information from a bus controller, wherein the first block size information defines a first amount of data to be output by the memory device onto a bus in response to a read request; receiving a first request from the bus controller; and outputting the first amount of data corresponding to the first block size information, in response to the first read request, onto the bus synchronously with respect to the external clock signal.	This claim is invalid as anticipated and/or rendered obvious by many prior art references, including without limitation the Bajwa, SCI, Fischer, Bomba, Penzel, Jackson, MC88200 and MIPS R6020 references. To the extent that Rambus's infringement contentions are premised on the term "bus" as not being limited to a multiplexed bus, the claim is also invalid under § 112 ¶ 1 for failure to meet the written description requirement.
19. The method of claim 18 further including: receiving a second read request from the bus controller, and outputting the first amount of data corresponding to the first block size information, in response to the second read request, onto the bus synchronously with respect to the external clock signal.	Same grounds as discussed for claim 18.
20. The method of claim 18 wherein first block size information further defines a first amount of data to be input by the memory device from the bus in response to a write request, the method further including: receiving a first write request from the bus controller, and	Same grounds as discussed for claim 18.

Claims of the '918 Patent	Grounds for Invalidity
inputting the first amount of data corresponding to the first block size information, in response to the first write request, from the bus synchronously with respect to the external clock signal.	
24. The method of claim 18 further including storing a delay time code in an access time register, the delay time code being representative of a number of clock cycles to transpire before data is output onto the bus after receipt of a read request and wherein the first amount of data corresponding to the first block size information is output in accordance with the delay time code.	Same grounds as discussed for claim 18.
25. The method of claim 24 wherein the delay time code is stored in the access time register after power is applied to the memory device.	Same grounds as discussed for claim 18.
29. The method of claim 18 wherein the first block size information is a binary representation of the first amount of data to be output after receipt of the first read request.	Same grounds as discussed for claim 18.
30. The method of claim 18 wherein the first block size information is indicative of an amount of data corresponding to one of a plurality of page mode accesses.	Same grounds as discussed for claim 18.
31. The method of claim 18 wherein the external clock signal has a fixed frequency and wherein the first amount of data corresponding to the first block size information is output synchronously during a plurality of clock cycles of the external clock signal.	Same grounds as discussed for claim 18.
32. The method of claim 31 further including automatically precharging the synchronous memory device after executing the first read request.	This claim is invalid as anticipated and/or rendered obvious by the Bajwa reference, or by combinations of a prior art reference taken from Group I below with a prior art reference taken from group II below: • Group I: SCI, Bajwa, Fischer, Bomba, Penzel, Jackson, MC88200, MIPS R6020 • Group II: Bajwa, Chin Same grounds for invalidity under § 112 ¶ 1 as in the independent claim.
33. The method of claim 18 further including generating at least one internal clock signal using a delay locked loop and the external clock signal wherein the first amount of data corresponding to the first block size information is output onto the bus synchronously with respect to at least one internal clock signal.	This claim is invalid as anticipated and/or rendered obvious by many prior art references, taken singly (e.g., SCI) or in combination, including without limitation combinations of a prior art reference taken from Group I below with a prior art reference taken from group II below: • Group I: SCI, Fischer, Bomba, Penzel, Jackson, MIPS R6020

Claims f the '918 Patent	Grounds for Invalidity
	• Group II: Flora, Uvieghara, Johnson I, Johnson II, Johnson III, MIPS R2010, MIPS R3010, Grover, Wiggers, Lofgren, SCI, MC88200 To the extent that Rambus's infringement contentions are premised on the term "bus" as not being limited to a multiplexed bus, the claim is also invalid under § 112 ¶ 1 for failure to meet the written description requirement. The claim is also invalid under § 112 ¶ 1 (written description, enablement) because the clock averaging feature (disclosed in Figs 8a/b and 12 of the patent specification) is not claimed, there is no disclosure of the use of a single clock signal transmitted as a single-ended signal or differentially, and/or because there is no disclosure of a "delay locked loop."
34. A method of operation of a synchronous memory device, wherein the memory device includes a plurality of memory cells and a time delay register, the method of operation of the memory device comprises: storing a value in the time delay register, the value being representative of a number of external clock cycles to transpire after which the memory device responds to a read request; receiving an external clock signal wherein the external clock signal has a fixed frequency; receiving block size information from a bus controller, wherein the block size information defines a first amount of data to be output by the memory device onto the bus in response to a read request; receiving a first read request from the bus controller; outputting the first amount of data corresponding to the block size information onto the bus in response to the first read request, wherein the memory device outputs the data synchronously with respect to the external clock signal, during a plurality of clock cycles of the external clock signal and in accordance with the value stored in the time delay register.	This claim is invalid as anticipated and/or rendered obvious by many prior art references, including without limitation the Bajwa reference, and by combinations of a prior art reference taken from Group I below with a prior art reference taken from group II below: • Group I: Bajwa, SCI, Fischer, Bomba, Penzel, Jackson, MC88200 and MIPS R6020 • Group II: Saccardi, Gigabit, Bajwa, Kawamesa, Hasegawa, Yamaguchi, White Same grounds for invalidity under § 112 ¶ 1 as in the independent claim.

INVALIDITY OF THE '195 PATENT

Claims of the '195 Patent	Grounds for Invalidity
1. A synchronous semiconductor memory device having at least one memory section including a plurality of memory cells, the memory device comprising: clock receiver circuitry to receive an external clock signal; a register which stores a value which is representative of a delay time after which the memory device responds to a read request; and a plurality of output drivers to output data after the delay time transpires and synchronously with respect to the external clock signal.	**1. Grounds for Invalidity Under Rambus's Infringement Contentions:** Under Rambus' infringement contentions, this claim is invalid as anticipated and/or rendered obvious by many prior art references, taken singly or in combination, including without limitation, the Saccardi, Gigabit, Bajwa, Kawamesa, Hasegawa, Yamaguchi and White references. To the extent that Rambus's infringement contentions are premised on the term "bus" as not being limited to a multiplexed bus, the claim is also invalid under § 112 ¶ 1 for failure to meet the written description requirement. **2. Grounds for Invalidity Under the Virginia Court's Claim Construction of the "bus" and "request" claim terms:** Alternatively, under the Virginia Court's claim construction, this claim is invalid as rendered obvious by many prior art references, taken singly or in combination, including without limitation, the combinations of any prior art reference taken from Group I below with any other prior art reference taken from Group II below: • Group I: Saccardi, Gigabit, Bajwa, Kawamesa, Hasegawa, Yamaguchi, White • Group II: Hoff, Fischer, MIPS R6020, Bomba, Penzel, Jackson **3. Additional § 112 ¶ 1 Grounds for Invalidity Under Either Rambus's Infringement Contentions or the Virginia Court's Claim Construction:** The claim is also invalid under § 112 ¶ 1 (written description, enablement) under either Rambus's infringement contentions or the Virginia Court's claim construction because there is no written support in the description for a claim that does not use the disclosed clock averaging feature (Figs 8a/b and 12 of the patent specification), and/or because there is no disclosure of the use of a single clock signal transmitted as a single ended signal or differentially.
2. The memory device of claim 1 further including: clock generation circuitry, coupled to the clock	Same grounds as discussed for claim 1.

Claims of the '195 Patent	Gr unds for Invalidity
receiver circuitry, t generate at least one internal clock signal; and wherein the plurality of output drivers output data in response to the internal clock signal.	
3. The memory device of claim 1 wherein the plurality of output drivers output data in response to a rising edge of the external clock signal.	Same grounds as discussed for claim 1.
4. The memory device of claim 1 further including: a delay locked loop, coupled to the clock receiver circuitry, to generate an internal clock signal using at least the external clock signal; and wherein the plurality of output drivers output data in response to the internal clock signal.	**1. Grounds for Invalidity Under Rambus's Infringement Contentions:** Under Rambus' infringement contentions, this claim is invalid as rendered obvious by many prior art references, taken singly or in combination, including the combination of any prior art reference from Group I below with any prior art reference from Group II below: • Group I: Saccardi, Gigabit, Bajwa, Kawamesa, Hasegawa, Yamaguchi, White • Group II: Grover, Flora, Uvieghara, Johnson I, Johnson II, Johnson III, MIPS R2010, MIPS R3010, Wiggers, Lofgren, SCI, MC88200 To the extent that Rambus's infringement contentions are premised on the term "bus" as not being limited to a multiplexed bus, the claim is also invalid under § 112 ¶ 1 for failure to meet the written description requirement. **2. Grounds for Invalidity Under the Virginia Court's Claim Construction of the "bus" and "request" claim terms:** Alternatively, under the Virginia Court's claim construction, this claim is invalid as rendered obvious by many prior art references, taken singly or in combination, including without limitation, any combination of three prior art references, each taken respectively from one of the Groups I, II or III below: • Group I: Saccardi, Gigabit, Bajwa, Kawamesa, Hasegawa, Yamaguchi, White • Group II: Grover, Flora, Uvieghara, Johnson I, Johnson II, Johnson III, MIPS R2010, MIPS R3010, Wiggers, Lofgren, SCI, MC88200 • Group III: Hoff, Fischer, MIPS R6020, Bomba, Penzel, Jackson **3. Additional § 112 ¶ 1 Grounds f r Invalidity Under Either Rambus's Infringement**

Claims f the '195 Patent	Grounds for Invalidity
	C ntentions or the Virginia C urt's Claim Constructi n: The claim is also invalid under § 112 ¶ 1 (written description, enablement) because the clock averaging feature (disclosed in Figs 8a/b and 12 of the patent specification) is not claimed, there is no disclosure of the use of a single clock signal transmitted as a single-ended signal or differentially, and/or because there is no disclosure of a "delay locked loop."
5. The memory device of claim 1 wherein the value which is representative of the delay time is stored in the register after power is applied to the device.	Same grounds as discussed for claim 1.
6. The memory device of claim 1 wherein the value stored in the register is representative of one of a plurality of different delay times.	Same grounds as discussed for claim 1.
7. The synchronous memory device of claim 1 wherein the value is representative of a number of clock cycles of the external clock.	Same grounds as discussed for claim 1.
8. The memory device of claim 7 wherein the value which is representative of the delay time is stored in the register after power is applied to the device.	Same grounds as discussed for claim 1.
9. The memory device of claim 8 further including: a delay locked loop, coupled to the clock receiver circuitry, to generate an internal clock signal using at least the external clock signal; and wherein the plurality of output drivers output data in response to the internal clock signal.	Same grounds as discussed for claim 4.
10. The memory device of claim 8 wherein the value stored in the register is representative of one of a plurality of different delay times.	Same grounds as discussed for claim 1.
11. A synchronous semiconductor memory device having at least one memory section including a plurality of memory cells, the memory device comprising: clock receiver circuitry to receive an external clock signal; at least one register to store a value which is representative of a delay time; and wherein in response to a read request, the memory device outputs data after the delay time transpires and synchronously with respect to the external clock signal.	Same grounds as discussed for claim 1.

Claims of the '195 Patent	Grounds f r Invalidity
12. The memory device of claim 11 further including: clock generation circuitry, coupled to the clock receiver circuitry, to generate an internal clock signal; and an output driver, coupled to the internal clock generation circuitry, to output the data in response to the internal clock signal.	Same grounds as discussed for claim 1.
13. The memory device of claim 12 wherein the output driver outputs data in response to a rising edge of the internal clock signal.	Same grounds as discussed for claim 1.
14. The memory device of claim 11 further including a delay locked loop, coupled to the clock receiver circuitry, to generate an internal clock signal using at least the external clock signal and wherein the output driver outputs data in response to the internal clock signal.	Same grounds as discussed for claim 4.
15. The memory device of claim 11 wherein the memory device, in response to a control register access, stores a value in the at least one register.	Same grounds as discussed for claim 1.
16. The memory device of claim 11 wherein the value stored in the register is representative of one of a plurality of available delay times.	Same grounds as discussed for claim 1.
17. The synchronous memory device of claim 11 wherein the value is representative of a number of clock cycles of the external clock signal.	Same grounds as discussed for claim 1.
18. The memory device of claim 17 wherein the value which is representative of the delay time is stored in the register after power is applied to the device.	Same grounds as discussed for claim 1.
19. The memory device of claim 17 further including: a delay locked loop, coupled to the clock receiver circuitry, to generate an internal clock signal using at least the external clock signal; and wherein the plurality of output drivers output data in response to the internal clock signal.	Same grounds as discussed for claim 4.
20. The memory device of claim 17 wherein the memory device outputs data in response to a rising edge of the external clock signal.	Same grounds as discussed for claim 1.

Claims of the '195 Patent	Grounds for Invalidity
21. The memory device of claim 20 further including: clock generation circuitry, coupled to the clock receiver circuitry, to generate an internal clock signal; and an output driver, coupled to the internal clock generation circuitry, to output the data in response to the internal clock signal.	Same grounds as discussed for claim 1.
22. The memory device of claim 21 wherein the output driver outputs data in response to a rising edge of the internal clock signal.	Same grounds as discussed for claim 1.
23. A method of controlling a synchronous memory device having at least one memory section including a plurality of memory cells and a register for storing a value which is representative of a time delay after which the memory device responds to a read request, the method comprising: issuing a read request to the memory device; and receiving data from the memory device, in response to the read request, wherein the memory device outputs the data after the time delay transpires and synchronously with respect to an external clock signal.	Same grounds as discussed for claim 1.
24. The method of claim 23 further including issuing a control register access, wherein, in response to the control registers access, the memory device stores the value in the register.	Same grounds as discussed for claim 1.
27. The method of claim 23 further including: initializing the register in the memory device by issuing a control register access on the bus; and providing the value which is representative of the time delay.	Same grounds as discussed for claim 1.
32. The method of claim 23 wherein the value stored in the register is one of a plurality of available delay times.	Same grounds as discussed for claim 1.
33. The method of claim 23 wherein the external clock signal has a fixed frequency.	Same grounds as discussed for claim 1.
34. A synchronous semiconductor memory device having at least one memory section including a plurality of memory cells, the memory device comprising:	Same grounds as discuss d for claim 1.

Claims f the '195 Patent	Grounds for Invalidity
clock receiver circuitry to receive an external clock signal; a register which stores a value which is representative of a number of cycles of the external clock signal to transpire after which the memory device responds to receiving a request to provide data; and a plurality of output drivers to output data in response to receiving a request to provide data, wherein the data is provided after the number of cycles of the external clock signal represented by the value have transpired.	
35. The memory device of claim 34 wherein the plurality of output drivers output data synchronously with respect to a transition of the external clock signal.	Same grounds as discussed for claim 1.
36. The memory device of claim 34 further including input receiver circuitry, coupled to the bus, to receive the request to provide data, wherein the request to provide data is sampled from the bus synchronously with respect to the external clock signal.	Same grounds as discussed for claim 1.

ATTACHMENT A TO APPENDIX B

Aichelmann: U.S. Patent No. 4,845,664, "On-Chip BIT Reordering Structure," issued Jul. 4, 1989 to Aichelmann, et al., filed Sept. 15, 1986, and originally assigned to IBM Corp.
Bajwa: U.S. Patent No. 4,785,428, "Programmable Memory Array Control Signals," issued November 15, 1988 to Bajwa, et al., and originally assigned to Intel Corporation.
Bomba: U.S. Patent No. 4,763,249, "Bus Device For Use In A Computer System Having A Synchronous Bus," issued Aug. 9, 1988 to Bomba, et al., and originally assigned to Digital Equipment Corporation.
Chappell: U.S. Patent No. 4,845,677, "Pipeline Memory Chip Structure Having Improved Cycle Time," issued Jul. 4, 1989 to Chappel, et al., and originally assigned to IBM Corp.
Chin: U.S. Patent No. 4,754,433, "Dynamic RAM Having Multiplexed Twin I/O Line Pairs," issued Jun. 28, 1988 to Chin, et al., and originally assigned to IBM Corp.
Fischer: U.S. Patent No. 4,785,394, "Fair Arbitration Technique For A Split Transaction Bus In A Multiprocessor Computer System," issued Nov. 15, 1988 to Fischer, and originally assigned to Datapoint Corporation.
Flora: U.S. Patent No. 4,637,018, "Automatic Signal Delay Adjustment Method," issued Jan. 13, 1987 to Flora, et al., and originally assigned to Burroughs Corporation.
Gigabit: GigaBit Logic 12G014 datasheet "256x4 Bit Registered, Self-Timed Static RAM, 2.5 ns Cycle Time," Aug. 1989 GaAs IC Data Book & Designer's Guide.
Graham: (Gigabit Logic), "Pipelined static RAM endows cache memories with 1-ns speed," Electronic Design, Dec. 1984.

Grover: U.S. Patent No. 5,361,277, "Method and Apparatus for Clock Distribution and for Distributed Clock Synchronization," issued Nov. 1, 1994, filed Mar. 30, 1989, and claiming a foreign application priority date of Apr. 27, 1988 (Canada). Assignee: Alberta Comm. Research Center. Inventor: Grover.

Hasegawa: Japanese Patent Application Kokai Publication No. Sho 60-80193, published May 8, 1985.
Hoff: U.S. Patent No. 3,821, 715,"Memory System for a Multi-Chip Digital Computer, " issued June 28,1974 to Hoff, Jr et al.
Jackson: U.S. Patent No. 4,315,308, "Interface Between A Microprocessor Chip And Peripheral Subsystems," issued Feb. 9, 1982 to Jackson, and originally assigned to Intel Corporation
Jeong: "Design of PLL-Based Clock Generation Circuits," IEEE Journal of Solid-State Circuits, Apr. 1987

Johnson is any one of the following references:

Johnson I - "A Variable Delay Line PLL for CPU-Coprocessor Synchronization," M. Johnson and E. Hudson, 1988 IEEE International Solid State Circuits Conference, Feb. 18, 1988.
Johnson II - IEEE paper, "A Variable Delay Line PLL for CPU-Coprocessor Synchronization," IEEE Journal of Solid-State Circuits, Oct. 1988.
Johnson III - U.S. Patent No. 5,101,117 to Johnson, priority date: Feb 17, 1988.

Kawamesa: Japanese Patent Application Kokai Publication No. S56-82961, Published July 7, 1981
Lofgren: U.K. Patent Application 2,197,553A, "Phase-locked Loop Delay Line," issued May 18, 1988 to Lofgren, et al., and originally assigned to Western Digital Corporation

MIPS R6020 is the bus architecture and bus controller chip for the MIPS R6000 system and family of products, as described in any of the following articles:

R6020 A - "R6000 System Bus & R6020 SBC Specification," MIPS Computer Systems, Inc., Aug. 22, 1989 (SGI0001598-1662).
R6020 B - "ECL Bus Controller Hits 266 Mbytes/s: MIPS R6020 Handles CPU, RAM, I/O Interface," M. Thorson, Microprocessor Report, v. 4, no. 1, Jan. 24, 1990.

M torola MC88200L: "Cache/Memory Management Unit User's Manual," published in 1988.

Penzel: U.S. Patent No. 4,394,753, "Integrated Memory Module Having Selectable Operating Functions," issued July 19, 1983 to Penzel, originally assigned to Siemens Aktiengesellschaft
Pinkham: "A High Speed Dual Port Memory with Simultaneous Serial and Random Mode Access for Video Applications," IEEE J. Solid-State Circuits, Dec. 1984.
Redwine: U.S. Patent No. 4,330,852, "Semiconductor Read/Write Memory Array Having Serial Access," issued May 18, 1982, to Redwine, et al., and originally assigned to Texas Instruments Incorporated
Saccardi: U.S. Patent No. 4,858,113, "Reconfigurable Pipelined Processor," issued Aug. 15, 1989; filed Apr. 10, 1987. Assignee: USA. Inventor: Saccardi.

SCI is the Scalable Coherent Interface technology described in the following articles:

SCI A – David B. Gustavson et al., "The Scalable Coherent Interface Project (Superbus), Aug. 22, 1988
SCI B – David B. Gustavson, "Scalable Coherent Interace", Nov. 1988
SCI C – Knut Alnes, "SCI: A Proposal For SCI Operation", Nov. 1988
SCI D – Knut Alnes, "SCI: A Proposal For SCI Operation", Jan. 1989
SCI E – Bjorn O. Bakka et al., "SCI: Logical Level Proposals", Jan. 1989
SCI F – Ernst H. Kristiansen et al, "Scalable Coherent Interface", Feb. 1989
SCI G – Morten Schanke, "Proposal For Clock Distribution In SCI", May 1989
SCI H – Ernst H. Kristiansen et al., "Scalable Coherent Interface, Eurobus, London", Sept 1989
SCI I – Richard A. Volz, et al., "Position Paper On Global Clock For The FutureBus +", 1989

Tam: U.S. Patent 4,680,738, "Memory With Sequential Mode," issued Jul. 15, 1987, to Tam, originally assigned to Advanced Micro Devices, Inc.
Uvieghara: "An On-Chip Smart Memory for a Data-Flow CPU," Uvieghara et al., IEEE J. Solid-State Circuits, Feb. 1990
Yamaguchi: Japanese Patent Application Sho 62-71428, "Semiconductor Memory Device," published October 5, 1988 toYamaguchi , originally assigned to Hitachi, Ltd.
White: U.S. Patent No. 5,140,688, "GaAs Integrated Circuit Programmable Delay Line Element," issued Aug. 18, 1992, claiming a US parent priority date of Nov. 10, 1986. Assigned to Texas Instruments. Inventor: White et al. Corresponds to Japanese patent JP 63-220637, published Sept. 1988.
Wiggers: U.S. Patent No. 4,998,262, "Generation of Topology Independent Reference Signals," issued Mar. 5, 1991; filed Oct. 10, 1989. Assignee: Hewlett-Packard. Inventor: Wiggers.

Appendix C - Micron Technology's Proposed Claim Construction of Certain Disputed Claim Terms

Claim Term	Meaning and Support
"Bus"	**Meaning:** The term "bus" means "a multiplexed set of signal lines used to transmit address, data and control information." This construction is identical to the Virginia Court's construction of the term "bus," (*Markman* Op. at 41), which is binding on Rambus in this case under the doctrine of collateral estoppel. **Support:** • The Virginia Court's *Markman* Opinion, e.g., pp. 15-41. • The Virginia Court's May 29, 2001 Supplemental Opinion, e.g., pp. 4-10. • The '918 patent specification, see, e.g., and without limitation 2:31-34, 2:43-49, 3:14-21, 3:50-4:13, 5:29-46, 5:59-64, 8:16-25, 14:49-67, 16:11-21, 24:37-42, and Fig. 2. • The file histories of all patents and patent applications that spring from the 1990 S/N 07/510,898 application, including without limitation the 150 original claims filed.
"Read Request"	**Meaning:** The term "read request" means "a series of bits transmitted over the bus that contain multiplexed address and control information needed to request a read of data from a memory device." This construction is identical to the Virginia Court's construction of the term "read request," (*Markman* Op. at 62), which is binding on Rambus in this case under the doctrine of collateral estoppel. **Support:** • The Virginia Court's *Markman* Opinion, e.g., pp. 47-62. • The Virginia Court's May 29, 2001 Supplemental Opinion, e.g., pp. 11-13. • Claims with any of the "request" claim terms. • The '918 patent specification, see, e.g., and without limitation 3:35-39, 4:9-11, 6:60-63, 8:24-29, 8:43-57, 8:59-9:4, 9:11-23, 12:4-16, 12:28-30, and Fig. 4. • The file histories of all patents and patent applications that spring from the 1990 S/N 07/510,898 application, including without limitation the 150 original claims filed.
"Write Request"	**Meaning:** The term "write request" means "a series of bits transmitted over the bus that contain multiplexed address and control inf rmation needed to request a write of data to a memory device." This construction is identical to the Virginia Court's construction of the term "write request," (*Markman* Op. at 62), which is binding on Rambus in this case

Claim Term	Meaning and Support
	under the doctrine of collateral estoppel. **Support:** • The Virginia Court's *Markman* Opinion, e.g., pp. 47-62. • The Virginia Court's May 29, 2001 Supplemental Opinion, e.g., pp. 11-13. • Claims with any of the "request" claim terms. • The '918 patent specification, see, e.g., and without limitation 3:35-39, 4:9-11, 6:60-63, 8:24-29, 8:43-57, 8:59-9:4, 9:11-23, 12:4-16, 12:28-30, and Fig. 4. • The file histories of all patents and patent applications that spring from the 1990 S/N 07/510,898 application, including without limitation the 150 original claims filed.
"Transaction Request"	**Meaning:** The term "transaction request" means "a series of bits transmitted over the bus that contain multiplexed address and control information needed to perform a transaction over the bus with a memory device." This construction is identical to the Virginia Court's construction of the term "transaction request," (*Markman* Op. at 62), which is binding on Rambus in this case under the doctrine of collateral estoppel. **Support:** • The Virginia Court's *Markman* Opinion, e.g., pp. 47-62. • The Virginia Court's May 29, 2001 Supplemental Opinion, e.g., pp. 11-13. • Claims with any of the "request" claim terms. • The '918 patent specification, see, e.g., and without limitation 3:35-39, 4:9-11, 6:60-63, 8:24-29, 8:43-57, 8:59-9:4, 9:11-23, 12:4-16, 12:28-30, and Fig. 4. • The file histories of all patents and patent applications that spring from the 1990 S/N 07/510,898 application, including without limitation the 150 original claims filed.
"Block Size"	**Meaning:** The term "block size" means "information that specifies the total amount of data that is to be transferred on the bus in response to a transaction request." This construction is identical to the Virginia Court's construction of the term "block size," (*Markman* Op. at 47), which is binding on Rambus in this case under the doctrine of collateral estoppel. **Support:** • The Virginia Court's *Markman* Opinion, e.g., pp. 41-47. • Claims with the "block size" claim term. • The '918 patent specification, see, e.g., and without limitation 3:21-26, 4:15-19, 11:41-63, and Fig. 4. • The file histories of all patents and patent applications that spring from the 1990 S/N 07/510,898 application, including without limitation the 150 original claims filed.

Claim Term	Meaning and Support
"First External Clock Signal"	**Meaning:** The term "first external clock signal" means "a periodic signal received by the memory device from an external source to provide first timing information." This construction is identical to the Virginia Court's construction of the term "first external clock signal," (*Markman* Op. at 69-70), which is binding on Rambus in this case under the doctrine of collateral estoppel. **Support:** • The Virginia Court's *Markman* Opinion, e.g., pp. 62-70. • Claims with any "external clock signal" claim term. • The '918 patent specification, see, e.g., and without limitation 3:27-29, 8:29-30, 18:63-19:32, 22:50-56, Fig. 8a, and Fig. 8b.
"Second External Clock Signal"	**Meaning:** The term "second external clock signal" means "a periodic signal received by the memory device from an external source to provide second timing information that is different from the first timing information." This construction is identical to the Virginia Court's construction of the term "second external clock signal," (*Markman* Op. at 70), which is binding on Rambus in this case under the doctrine of collateral estoppel. **Support:** • The Virginia Court's *Markman* Opinion, e.g., pp. 62-70. • Claims with any "external clock signal" claim term. • The '918 patent specification, see, e.g., and without limitation 3:27-29, 8:29-30, 18:63-19:32, 22:50-56, Fig. 8a, and Fig. 8b.
"Integrated Circuit Device"	**Meaning:** An "integrated circuit device" must have a device ID register, interface circuitry and comparison circuitry. This construction is identical to the Virginia Court's construction of the term "integrated circuit device," (*Markman* Op. at 74), which is binding on Rambus in this case under the doctrine of collateral estoppel. **Support:** • The Virginia Court's *Markman* Opinion, e.g., pp. 70-74. • The '918 patent specification, see, e.g., and without limitation 3:50-60, 4:20-25, 5:42-44, 6:28-66, 7:56-63, 8:30-34, 8:65-9:10, 10:4-8, 14:48-15:64, and Fig. 16. • The file histories of all patents and patent applications that spring from the 1990 S/N 07/510,898 application, including without limitation the 150 original claims filed and the file history of the '804 patent.